IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(Attorney Docket No. 18580US02)

In re: Ahmadreza Rofougaran **Electronically Filed on December 6, 2010**

Serial No.: 11/754,705

Filed: May 29, 2007

For: METHOD AND SYSTEM FOR CLOCKING FM TRANSMIT FM RECEIVE, AND NEAR FIELD COMMUNICATION FUNCTIONS USING DDFS

Examiner: Zhiyu Lu

Art Unit: 2618

Conf. No.: 7857

RESPONSE UNDER 37 C.F.R. § 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper responds to the non-final Office Action mailed on September 27, 2010 ("Office Action") in the above-identified patent application ("Application"). This response is being timely filed within three months from the mailing date. The Applicant respectfully requests consideration of the following remarks.

Amendments to the Specification begins on page 2 of this paper.

Listing of the Claims begins on page 6 of this paper.

Remarks/Arguments begin on page 11 of this paper.

AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

[0002] This application also makes reference to:

United States Patent Application Serial No. 11/754,481, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18372US02) filed on even date herewith;~~

United States Patent Application Serial No. 11/754,460, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18574US02) filed on even date herewith;~~

United States Patent Application Serial No. 11/754,581, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18575US02) filed on even date herewith;~~

United States Patent Application Serial No. 11/754,621, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18576US02) filed on even date herewith;~~

United States Patent Application Serial No. 11/754,490, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18577US02) filed on even date herewith;~~

United States Patent Application Serial No. 11/754,708, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18578US02) filed on even date herewith;~~

United States Patent Application Serial No. 11/754,768, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18579US02) filed on even date herewith;~~

United States Patent Application Serial No. 11/754,600, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18581US02) filed on even date herewith;~~

United States Patent Application Serial No. 11/754,407, filed on May 29, 2007; [[_____]] ~~(Attorney Docket Number 18590US02) filed on even date herewith~~; and

United States Patent Application Serial No. 11/754,438, filed on May 29, 2007. [[_____]] ~~(Attorney Docket Number 18591US02) filed on even date herewith.~~

[0007] Mobile terminals that support audio applications are becoming increasingly popular and, consequently, there is a growing demand for various [[for]] audio communications applications. For example, some users may utilize Bluetooth-

enabled devices, such as headphones and/or speakers, to allow them to communicate audio data with their wireless handset while freeing them to perform other activities. Other users may have portable electronic devices that may enable them to play stored audio content and/or receive audio content via FM broadcast communication, for example. Other users may use mobile terminals that have near field communication (NFC) capability.

[0037] The DDFS 208 may generate at least one output signal that may be used as a LO signal for transmission and reception of RF signals by the FM transmitter 210. The DDFS 208 may generate, for example, I and Q LO signals for use by the FM transceiver 210. An output of the DDFS 208 may also be used, for example, as a reference clock for the DDFS 214. The reference clock for the DDFS 214 may be, for example, an I or Q LO signal generated by the DDFS 208. The output of the DDFS 214 may be used for transmission and reception of RF signals by the NFC transceiver 216.

[0048] In this manner, the output of the phase accumulator 302, which may be referred to as F_{out}, may be periodic at a period of $1/ F_{out}$ and may represent the phase angle of a signal. In this regard, the DDFS 300[[322]] may operate as a frequency generator that generates one or more sine waves or other periodic waveforms over a large range of frequencies, from almost DC to approximately half the reference clock frequency F_{ref}.

[0049] Prior to changing the input control word CTRL, the state of the DDFS 300 may be saved in, for example, a memory such as the system memory 158, described with respect to FIG. 1[[1A]]. In this manner, the output signal F_{out} may be interrupted and then resumed without losing the phase information comprising the generated signals. For example, the DDFS 300 may resume generating the output signal F_{out} using the saved state loaded from, for example, the system memory 158. Accordingly, the output signal F_{out} may resume from the last phase angle transmitted before the

signal was interrupted.

[0051] The reference oscillator 402[[404]] may comprise suitable logic and/or circuitry that may be adapted to generate a signal of a fixed frequency. The signal may be utilized as a reference signal for a phased lock loop circuit. This signal may be, for example, a low frequency signal on the order of megahertz or tens of megahertz. The phase detector 404 may comprise suitable logic and/or circuitry that may be adapted to compare two signals and generate an output voltage that may indicate whether the two signals have the same frequency, or whether the frequency of one signal may be larger than the frequency of the other signal.

[0055] FIG. 5 is a flow diagram illustrating exemplary steps for using direct digital frequency synthesizers with a plurality of communication protocols, in accordance with an embodiment of the invention. Referring to FIG. 5, there are[[is]] shown steps 500 to 506. In step 500, the PLL 204 may generate a BT frequency for use by the Bluetooth transceiver 202. In step 502, the BT frequency, which may be from 2.402 GHz to 2.480 GHz, may be divided to a lower frequency suitable for use by a DDFS. For example, the divider block 206 may provide a lower frequency signal by dividing the input signal from the PLL 204.

[0057] FIG. 6 is a flow diagram illustrating exemplary steps for using direct digital frequency synthesizers, in accordance with an embodiment of the invention. Referring to FIG. 6, there are[[is]] shown steps 600 to 604. In step 600, an input frequency may be determined. The input frequency determination may be made by a processor such as, for example, the baseband processor 154 and/or the processor 156. In step 602, a frequency control word may be determined for use by a DDFS to generate a desired output frequency. A processor such as, for example, the baseband processor 154 and/or the processor 156 may determine the proper output frequency. The frequency word control block 212 may then determine an appropriate frequency word control to

communicate to the appropriate DDFS. The frequency word may be based on, for example, the width in bits of the frequency word control block 212, the frequency of the reference clock for the appropriate DDFS, and the output frequency desired. In step 604, the frequency control word may be communicated to the appropriate DDFS.

THE CLAIMS

Claims 1-30 are pending in the instant application. Claims 1 and 16 are independent claims. Claims 2-15 and 17-30 depend from claims 1 and 16, respectively.

Listing of Claims:

1. (Original) A method for wireless communication, the method comprising:

generating a first signal used to process signals for Bluetooth transmission and/or reception;

clocking via a second signal derived from said first signal, a first direct digital frequency synthesizer (DDFS) to generate a first DDFS output signal to enable processing of signals for FM radio transmission and/or FM radio reception; and

clocking via said first DDFS output signal, at least a second DDFS to generate a second DDFS output signal to enable processing of signals to be transmitted using near field communication (NFC) protocol and/or processing received NFC protocol signals.

2. (Original) The method according to claim 1, wherein said first signal is generated via a local oscillator circuit.

3. (Original) The method according to claim 1, wherein said first signal is generated via a phase locked loop circuit.

4. (Original) The method according to claim 1, comprising generating one or more frequency control words that control generation of said first DDFS output signal and said second DDFS output signal.

5. (Original) The method according to claim 4, comprising simulating simultaneous transmission FM radio signals and reception of FM radio signals by switching said generated one or more frequency control words.

6. (Original) The method according to claim 4, comprising switching said generated one or more frequency control words, which control generation of said first DDFS output signal, between a plurality of values in successive time intervals to perform time division duplexing of said transmission of FM radio signals and said reception of FM radio signals.

7. (Original) The method according to claim 4, comprising adjusting said generated one or more frequency control words, which control said generation of said first DDFS output signal to compensate for changes in a frequency of said first signal.

8. (Original) The method according to claim 4, comprising adjusting said generated one or more frequency control words, which control said generation of said second DDFS output signal to compensate for changes in a frequency of said first DDFS output signal.

9. (Original) The method according to claim 1, wherein said transmission of said FM radio signals occurs at a first frequency and said reception of FM radio signals occurs at a second frequency.

10. (Original) The method according to claim 1, comprising adjusting a frequency of said first signal for processing received Bluetooth signals or processing signals to be transmitted according to the Bluetooth protocol.

11. (Original) The method according to claim 1, wherein said first signal comprises an in-phase (I) component and a quadrature (Q) component.

12. (Original) The method according to claim 11, comprising clocking said first DDFS via one of said in-phase (I) component and said quadrature (Q) component.

13. (Original) The method according to claim 1, wherein said first DDFS output signal has constant frequency while said first signal varies in frequency.

14. (Original) The method according to claim 1, wherein said second DDFS output signal has constant frequency while said first DDFS output signal varies in frequency.

15. (Original) The method according to claim 1, wherein said second signal has a frequency equal to or less than said first signal.

16. (Original) A system for wireless communication, the system comprising:

one or more circuits on a chip that enables generation of a first signal used to process signals for Bluetooth transmission and/or reception; and

said one or more circuits generates from said first signal, a second signal which clocks a first direct digital frequency synthesizer (DDFS), which generates a first DDFS output signal to enable processing of signals to be transmitted using FM radio protocol and/or processing of received FM radio protocol signals; and

a second DDFS, clocked via said first DDFS output signal, which generates a second DDFS output signal to enable processing signals to be transmitted using near field communication (NFC) protocol and/or processing received NFC protocol signals.

17. (Original) The system according to claim 16, wherein said one or more circuits comprises a local oscillator circuit that generates said first signal.

18. (Original) The system according to claim 16, wherein said one or more circuits comprises a phase locked loop circuit that generates said first signal.

19. (Original) The system according to claim 16, wherein said one or more circuits enables generation of one or more frequency control words that control generation of said first DDFS output signal and said second DDFS output signal.

20. (Original) The system according to claim 19, wherein said one or more circuits enables simulated simultaneous transmission of FM radio signals and reception of FM radio signals by switching said generated one or more frequency control words.

21. (Original) The system according to claim 19, wherein said one or more circuits enables time division duplexing of said transmission of FM radio signals and said reception of FM radio signals by switching said generated one or more frequency control words, which control generation of said first DDFS output signal, between a plurality of values in successive time intervals.

22. (Original) The system according to claim 19, wherein said one or more circuits enables adjustment of said generated one or more frequency control words to control said generation of said first DDFS output signal to compensate for changes in a frequency of said second signal.

23. (Original) The system according to claim 19, wherein said one or more circuits enables adjustment of said generated one or more frequency control words to control said generation of said second DDFS output signal to compensate for changes in a frequency of said first DDFS output signal.

24. (Original) The system according to claim 16, wherein said one or more circuits enables transmission of said FM radio signals occurs at a first frequency and said reception of FM radio signals occurs at a second frequency.

25. (Original) The system according to claim 16, wherein said one or more circuits enables adjustment of a frequency of said first signal for processing received Bluetooth signals or processing signals to be transmitted according to the Bluetooth protocol.

26. (Original) The system according to claim 16, wherein said first signal comprises an in-phase (I) component and a quadrature (Q) component.

27. (Original) The system according to claim 26, wherein said first DDFS is clocked via one of said in-phase (I) component and said quadrature (Q) component.

28. (Original) The system according to claim 16, wherein said first DDFS output signal has constant frequency while said first signal varies in frequency.

29. (Original) The system according to claim 16, wherein said second DDFS output signal has constant frequency while said first DDFS output signal varies in frequency.

30. (Original) The system according to claim 16, wherein said second signal has a frequency equal to or less than said first signal.

REMARKS/ARGUMENTS

The present application includes pending claims 1-30, all of which have been rejected. The Applicant respectfully submits that the claims define patentable subject matter.

Claims 1-3, 10-18, and 25-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Frerking et al. (US 7,620,429), hereinafter Frerking, in view of Liao (US 2005/0090208), hereinafter Liao. Claims 4-8 and 19-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Frerking in view of Liao and Gourse (US 5,598,437), hereinafter Gourse. Claims 9 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Frerking in view of Liao and Terreault (US 6,058,292), hereinafter Terreault.

The Applicant respectfully traverses these rejections at least for the reasons previously set forth during prosecution and at least based on the following remarks.

REJECTION UNDER 35 U.S.C. § 103

The MPEP states the following regarding the requirements for establishing a *prima facie* case of obviousness:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

See the MPEP at § 2142, citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006), and *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" *See id.,* § 2143.01. Furthermore, in order to render the claims obvious, the asserted prior art combination must **teach or suggest each and <u>every</u> claim feature**. *See In re Royka*, 490 F.2d 981 (CCPA 1974) (to establish *prima facie* obviousness of a claimed invention, all the claim features must be taught or suggested by the prior art)[1]; *see also In re Wada and Murphy*, Appeal 2007-3733, citing *In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (A proper obviousness determination requires that an Examiner make "a searching comparison of the claimed invention – **including all its limitations** – with the teaching of the prior art.")

If a *prima facie* case of obviousness is not established, the Appellant has no obligation to submit evidence of nonobviousness:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

With these principles in mind, the Applicants now turn to the claim rejections in particular.

[1] Emphasis added except where noted otherwise.

I. The Proposed Combination of Frerking and Liao Does Not Render Claims 1-3, 10-18, and 25-30 Unpatentable

A. Independent Claims 1 and 16

With regard to the rejection of independent claim 16 under 35 U.S.C. § 103(a), the Applicant submits that the combination of Frerking and Liao does not disclose or suggest at least the limitation of "said one or more circuits generates from said first signal, a second signal which clocks a first direct digital frequency synthesizer (DDFS), which generates a first DDFS output signal to enable processing of signals to be transmitted using FM radio protocol and/or processing of received FM radio protocol signals; and a second DDFS, clocked via said first DDFS output signal, which generates a second DDFS output signal to enable processing signals to be transmitted using near field communication (NFC) protocol and/or processing received NFC protocol signals," as recited by the Applicant in independent claim 16.

The Office Action states the following:

> Regarding claim 16, Frerking et al. teach a system for wireless communication, the system comprising: one or more circuits on a chip that enables generation of a first signal used to process signals for Bluetooth transmission and/or reception (204 of Fig. 2); and said one or more circuits generates, a second signal to enable processing of signals to be transmitted using FM radio protocol and/or processing of received FM radio protocol signals (206 of Fig. 2, column 2 lines 29-44); and to enable processing signals to be transmitted using near field communication (NFC) protocol and/or processing received NFC protocol signals (206 of Fig. 2, column 2 lines 29-44, wherein module 206 facilitate both FM and NFC protocols).

See Office Action at page 2. The Applicant respectfully disagrees with this analysis. The Examiner refers for support to 204 and 206 of Fig. 2, and column 2, lines 29-44 of Frerking. With regard to 204 and 206 of Fig. 2, Frerking states the following:

> The HAS 100 also includes an Interface 104 for communicating with the BWCD 102. The Interface 104 includes an Interface Bluetooth Communications Module (IBCM) 204 that includes Bluetooth Circuitry for wirelessly exchanging signals with another Bluetooth-enabled device, such as the BWCD 102 substantially in accordance with the Bluetooth specification. Thus, the IBCM 204 allows the Interface 104 to establish a communications link with the BWCD 102 and receive signals transmitted from the BWCD 102 via a Bluetooth signal 112.The illustrated Interface 104 also includes means for short range communication, such as a Low Power RF Module 206. The Low Power RF Module 206 includes transceiver circuitry for establishing a communications link with the RHAD 106, and wirelessly exchanging analog or digitized audible signals with the RHAD 106 via a low power RF signal 114. The Interface 104 can further include a controller 208 having control logic for managing and controlling the BCM 204 and the Low Power RF Module 206.

See Frerking, col. 6, lines 16-34.

Col. 6, lines 16-34 of Frerking merely lists the capabilities of the Interface Bluetooth Communications Module (IBCM) 204 and the Low Power RF Module 206. With regard to the IBCM 204, Frerking only states that it "includes Bluetooth Circuitry for wirelessly exchanging signals with another Bluetooth-enabled device, such as the BWCD 102 **substantially in accordance with the Bluetooth specification**." *See* Frerking at col. 6, lines 19-22 (emphasis added). However, Frerking does not disclose **what** electrical components are used and **how** the underlying functionality is implemented. Similarly, with regard to the Low Power RF Module 206, Frerking merely states that it includes circuitry for establishing a communications link and exchanging signals with the RHAD 106 but does not disclose any further details regarding said circuitry.

With regard to both the IBCM 204 and the Low Power RF Module 206, Frerking does not disclose any direct digital frequency synthesizer (DDFS) or any signal which clocks a DDFS output signal. In other words, Frerking does not disclose or suggest "said

one or more circuits generates from said first signal, a second signal which clocks a first direct digital frequency synthesizer (DDFS), which generates a first DDFS output signal to enable processing of signals to be transmitted using FM radio protocol and/or processing of received FM radio protocol signals; and a second DDFS, clocked via said first DDFS output signal, which generates a second DDFS output signal to enable processing signals to be transmitted using near field communication (NFC) protocol and/or processing received NFC protocol signals," as recited by the Applicant in independent claim 16.

The Examiner also relies on col. 2, lines 29-44 of Frerking which states the following:

> While embodiments of the invention are described with regard to specific communication protocols and standards, such as Bluetooth, those skilled in the art will recognize that embodiments of the invention that are short range communication enabled may comprise a broad range of protocols or standards. Means for short range communication include IEEE 802.11, 802.15.1 (Bluetooth and Bluetooth lite), 802.15.4a (Zigbee), 802.15.3 (Ultra Wideband), IrDa, nearfield communications (NFC), active radio-frequency identification (active RFID), low power FM, propriety standards, and other low power wireless transceivers. Accordingly, although the illustrated embodiments teach the present invention by way of a Bluetooth protocol, this is for purposes of illustration only and not limitation as all means for short range communication are contemplated and many are shown immediately above.

See Frerking, col. 2, lines 29-44.

Col. 2, lines 29-44 of Frerking lists various means for short range communication. However, col. 2, lines 29-44 of Frerking does not disclose **what** electrical components are used and **how** the underlying functionality is implemented. Specifically, Frerking does not disclose any direct digital frequency synthesizer (DDFS) or any signal which clocks a DDFS. That is, Frerking does not disclose or suggest "said one or more circuits generates from said first signal, a second signal which clocks a first direct digital

frequency synthesizer (DDFS), which generates a first DDFS output signal to enable processing of signals to be transmitted using FM radio protocol and/or processing of received FM radio protocol signals; and a second DDFS, clocked via said first DDFS output signal, which generates a second DDFS output signal to enable processing signals to be transmitted using near field communication (NFC) protocol and/or processing received NFC protocol signals," as recited by the Applicant in independent claim 16.

The Examiner concedes (and the Applicant agrees) that "Frerking et al. do not expressly disclose the second signal is generated from said first signal, which clocks a first direct digital frequency synthesizer (DDFS), which generates a first DDFS output signal; and a second DDFS, clocked via said first DDFS output signal, which generates a second DDFS output signal." *See* Office Action at page 2. The Examiner relies on Liao to address this deficiency of Frerking. *See* Office Action at page 3.

The Office Action states:

> Liao teaches a multi-mode and multi-standard device (paragraph 0025) that generates/derives different signals for different standards from a single VCO generated signal (paragraph 0009), wherein f1 (Fig. 1) is generated (Fig. 4) and f3 is generated via DDFS (105 of Fig. 1, paragraph 0023) based on f1. It would have been obvious to one of ordinary skill in the art to recognize that the signals required by different standards of Frerking et al. could be derived in **linear hierarchy** with implementation of DDFS. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize Liao's teaching and modify the system of Frerking et al. into deriving **different signals** for FM and NFC **through different DDFS based** on a signal generated for Bluetooth by implementation design preference.

See Office Action at page 3 (emphasis added). The Applicant respectfully disagrees with this analysis.

> Liao states the following:
>
> As more communication standards are integrated into a single mobile device, the invention provides a single transceiver device to have multi-mode or multiple standard frequency channels access capability with **one single frequency synthesizer**.

See Liao, paragraph 0005 (emphasis added). As it may be seen from the above citation, Liao limits the invention to one **single** frequency synthesizer, without the use of a second synthesizer clocked by an output signal from the first synthesizer. In this regard, Liao does not disclose "said one or more circuits generates from said first signal, a second signal which clocks a first direct digital frequency synthesizer (DDFS), which generates a first DDFS output signal to enable processing of signals to be transmitted using FM radio protocol and/or processing of received FM radio protocol signals; **and a second DDFS, clocked via said first DDFS output signal**, which generates a second DDFS output signal to enable processing signals to be transmitted using near field communication (NFC) protocol and/or processing received NFC protocol signals," as recited by the Applicant in independent claim 16.

Furthermore, with regard to the potential use of even a single DDFS, Liao states the following:

> And the mixed-signal f3 waveform synthesizer can also be a direct digital frequency synthesizer (DDFS) circuits which need **more complicated design and power consumption**.

See Liao, paragraph 0023 (emphasis added). By citing "more complicated design and power consumption," Liao appears to discourage the use of DDFS circuits. That is, Liao arguably teaches away from DDFS.

Therefore, the combination of Frerking and Liao does not disclose or suggest "said one or more circuits generates from said first signal, a second signal which clocks a first direct digital frequency synthesizer (DDFS), which generates a first DDFS output signal to enable processing of signals to be transmitted using FM radio protocol and/or processing of received FM radio protocol signals; and a second DDFS, clocked via said first DDFS output signal, which generates a second DDFS output signal to enable processing signals to be transmitted using near field communication (NFC) protocol and/or processing received NFC protocol signals," as recited by the Applicant in independent claim 16. Consequently, the Applicant respectfully submits that the Examiner has not provided an "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" in the detailed manner described in *KSR*.

Accordingly, the Applicant maintains that the proposed combination of Frerking and Liao does not render independent claim 16 unpatentable, and a *prima facie* case of obviousness has not been established. The Applicant submits that claim 16 is allowable. Independent claim 1 is similar in many respects to the system disclosed in independent claim 16. Therefore, the Applicant submits that independent claim 1 is also allowable over the references cited in the Office Action at least for the reasons stated above with regard to claim 16.

B. Dependent Claims 2-3, 10-15, 17-18, and 25-30

Based on at least the foregoing, the Applicant believes the rejection of independent claims 1 and 16 under 35 U.S.C. § 103(a) as being anticipated by the combination of Frerking and Liao has been overcome and requests that the rejection be

withdrawn. Additionally, claims 2-3, 10-15, 17-18, and 25-30 depend from independent claims 1 and 16 respectively, and are consequently, also respectfully submitted to be allowable based on the above arguments. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 2-3, 10-15, 17-18, and 25-30.

II. The Proposed Combination of Frerking, Liao, and Gourse Does Not Render Claims 4-8 and 19-23 Unpatentable

Based on at least the foregoing, the Applicant believes the rejection of independent claims 1 and 16 under 35 U.S.C. § 103(a) as being anticipated by the combination of Frerking and Liao has been overcome and requests that the rejection be withdrawn. Additionally, since the additional cited reference (Gourse) does not overcome the deficiencies of Frerking and Liao, claims 4-8 and 19-23 which depend from independent claims 1 and 16 respectively, are consequently, also respectfully submitted to be allowable based on the above arguments. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 4-8 and 19-23.

III. The Proposed Combination of Frerking, Liao, and Terreault Does Not Render Claims 9 and 24 Unpatentable

Based on at least the foregoing, the Applicant believes the rejection of independent claims 1 and 16 under 35 U.S.C. § 103(a) as being anticipated by the combination of Frerking and Liao has been overcome and requests that the rejection be

withdrawn. Additionally, since the additional cited reference (Terreault) does not overcome the deficiencies of Frerking and Liao, claims 9 and 24 which depend from independent claims 1 and 16 respectively, are consequently, also respectfully submitted to be allowable based on the above arguments. The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 9 and 24.

In general, the Office Action makes various statements regarding claims 1-30 and the cited references, which statements are now moot in light of the above. Thus, the Applicant will not address such statements at the present time. However, the Applicant expressly reserves the right to challenge such statements in the future should the need arise (e.g., if such statement should become relevant by appearing in a rejection of any current or future claim).

CONCLUSION

Based on at least the foregoing, the Applicant believes that claims 1-30 are in condition for allowance. If the Examiner disagrees, the Applicant respectfully requests a telephone interview, and requests that the Examiner telephone the undersigned Attorney at 312-775-8000.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

A Notice of Allowability is courteously requested.

Respectfully submitted,

Date: December 6, 2010 /Athar A. Khan/

Athar A. Khan, Esq.
Registration No. 60271
Attorney for Applicant

MCANDREWS, HELD & MALLOY, LTD.
500 WEST MADISON STREET, 34TH FLOOR
CHICAGO, ILLINOIS 60661
(312) 775-8000 (AAK)